REMARKS

Applicant respectfully requests consideration of the present application in view of the foregoing amendments, the requests for continued examination and in view of the reasons which follow.

Claims 1-24 and 27-28 stand rejected in the Advisory Office Action dated January 29, 2003. Claims 1-12 have been amended. Claim 29 has been added. Accordingly, Claims 1-24 and 27-29 remain pending in the application.

In paragraphs 2 and 3 of the Final Office Action, claims 1-3 and 7-10 are rejected under 35 U.S.C. § 103 as being obvious over by U.S. Patent No. 5,591,653 (Sameshima). The Examiner states:

> Sameshima et al. discloses a method of manufacturing an integrated circuit, comprising; providing an amorphous semiconductor material 3 including ... above a bulk substrate of single crystal semiconductor material 100 al. [and] providing a cap layer 6 before the doping step.

Applicant respectfully traverses the rejection. In particular, applicant respectfully traverses the Examiner's conclusions that Sameshima discloses or suggests a bulk substrate.

In paragraph 4 of the Final Office Action, Claims 1-24, 27 and 28 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 5,461,250 (Burghartz) in view of Sameshima. The Examiner states:

> Burghartz et al. discloses a process of forming a transistor with a silicon germanium channel region, the process comprising; depositing a thin silicon germanium material above a top surface of a semiconductor substrate ... [and also] discloses forming silicide layers on the source and drain regions (see figure 4).

Applicant respectfully traverses the rejection. Burghartz and Sameshima are referred to below as the cited art.

With respect to claims 1-24 and 27-28, it is respectfully submitted that the combination of Sameshima and Burghartz would not cause one of ordinary skill in the

art to arrive at the present invention. Sameshima teaches an SOI substrate, which is conventional for thin film transistors. Substrate 1 of Sameshima is not a bulk substrate because it is manufactured of glass. Burghartz similarly builds its TFT on an insulator and only mentions the possibility of a silicon support substrate. Burghartz, column 6, lines 16-24. Even if a semiconductor support structure were utilized, the TFT would still be built on an insulative layer 114 that is necessary for gate insulation. Therefore, the cited art does not teach the bulk substrate of the present invention. Accordingly, it is respectfully submitted that Claims 1-24 and 27-28 are patentable over the cited art.

With respect to independent claim 27, the method dopes at least a portion of the bulk substrate to form the source and drain regions. Claim 27 recites:

> doping the single crystalline layer and the substrate at a source location and a drain location to form a source region and a drain region....

Such a feature allows deep source and drain regions to be formed with sufficient depth for silicidation and yet achieve a thin channel region including germanium. See present application, page 9, lines 15-16.

The doping feature of claim 27 is not shown, described or suggested in the cited art. In Sameshima, semiconductor substrate capable of being doped for source and drain regions is not mentioned or suggested. Similarly, Burghartz does not discuss or suggest doping a bulk substrate. Indeed, with the preferred SOI architecture of the cited art, the bulk substrate doping would not be possible. Accordingly, it is respectfully submitted that Claim 27 and its dependent Claim 28 are additionally patentable over the cited art.

With respect to independent claim 1, dependent claim 11, dependent claim 28 and dependent claim 29, the depth of the silicide layer and/or the function of reducing the effects of germanium in the source regions is recited. Such a feature is described in the detailed description of the present application. The present application states:

> Siliciding regions 22 and 24 to form regions 82 can consume the portion of regions 22 and 24 that includes germanium.... Thus,

the performance of regions 22 and 24 is not adversely impacted by the presence of germanium.

See present application, page 7, lines15-18. Thus, the features of Claims 1, 11, 28 and 29 provide significant advantages.

The features of Claims 1, 11, 28, and 29 are not shown, described or suggested in the cited art. In Sameshima, silicide layers are not even mentioned, much less the particular depth for the silicide with respect to another layer. Although Burghartz discloses a silicide layer, there is no discussion of that layer being deeper than layer 102. In fact, Burghartz does not even discuss a preferred thickness for the silicide layers. See Burghartz, column 9, lines 33-36. Accordingly, it is respectfully submitted that Claims 1,11, 28, and 29 and 28 are additionally patentable over the cited art.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 2-24-03

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MARKED UP VERSION

In The Claims:

1. (Twice Amended) A method of manufacturing an integrated circuit, comprising:

providing an amorphous semiconductor material including germanium above a bulk substrate of semiconductor material;

laser annealing the amorphous semiconductor material to form a single crystalline semiconductor layer containing germanium; [and]

doping the single crystalline semiconductor layer and the substrate at a source location and a drain location to form a source region and a drain region, whereby a channel region between the source region and the drain region includes a thin semiconductor germanium region; and

siliciding the source region and the drain region to form a silicide layer, the silicide layer extending into the substrate.

11. (Thrice Amended) The method of claim 1, further comprising:

providing a second amorphous semiconductor material above the amorphous semiconductor material including germanium [before] after the laser annealing step, [wherein the] performing another laser annealing step [forms] to form a second single crystalline semiconductive layer from the second amorphous semiconductor material; and

wherein the siliciding step forms the silicide layer [the source region and the drain region to form a silicided layer wherein] so that the depth of the silicided layer is deeper than the second single crystalline semiconductor layer.

12. (Twice Amended) A method of manufacturing an ultra-large scale integrated circuit including a transistor, the method comprising steps of:

depositing an amorphous silicon germanium material above a top surface of a semiconductor substrate;

first annealing the amorphous silicon germanium material;

depositing an amorphous silicon material above the silicon germanium material;

second annealing the amorphous silicon material; and

providing a source region and a drain region for the transistor, the source region and the drain region being deeper than a combined thickness of the silicon germanium material and the silicon material.